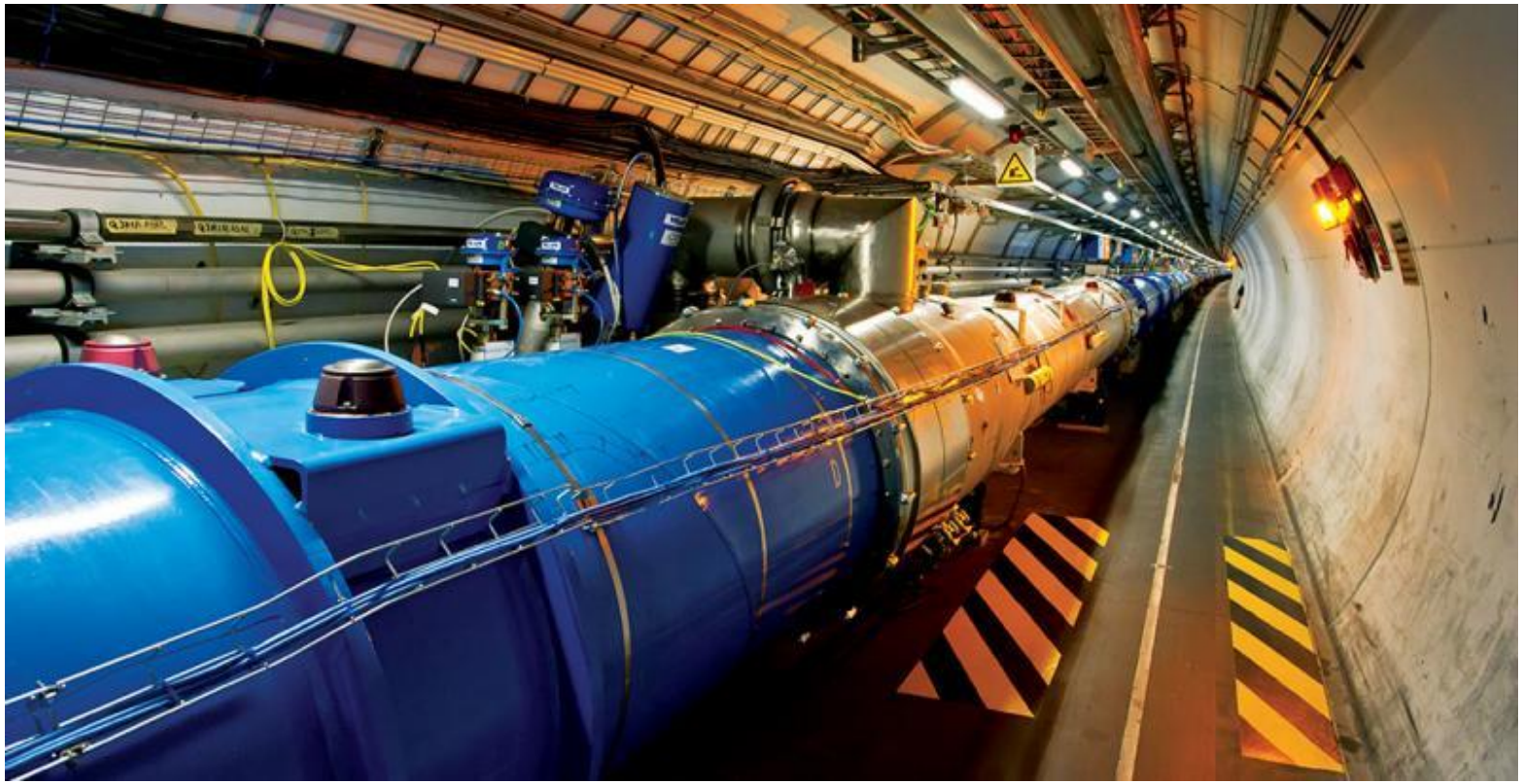


High DR ADC for LHC

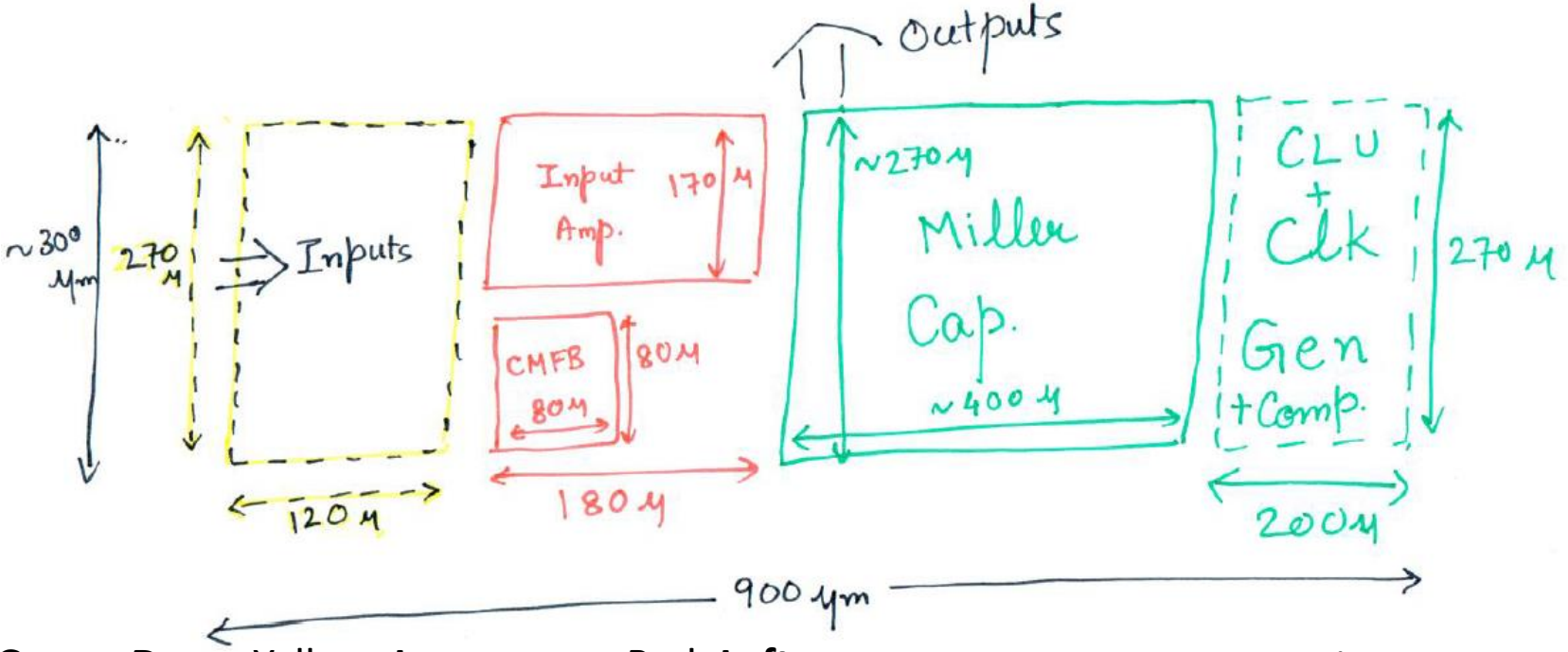
Sarthak Kalani

Last updated: 04/14/17

COLUMBIA UNIVERSITY
IN THE CITY OF NEW YORK

Columbia Integrated Systems Laboratory

Layout Status update



- Green: **Done**, Yellow: **In-progress**, Red: **Left**
- Total **area** anticipated: 950um x 300um
- Timeline:
  - Finish Individual blocks by Tuesday
  - Complete Chip routing by **April 22nd**
- **Some challenges** (faced/to remember):
  - Mim Cap: Different errors when area grows bigger
  - Mim Cap: Using 2 terminal now. -> Need Pex Sims

Timing Issue: Resolved?

- SAR samples when DRE output is being held: Output will not be ready by then based on current scheme